Amendments to the Claims

1. (*Cancelled*)

2. (*Currently Amended*) ~~A semiconductor device as claimed in Claim 1,~~ The semiconductor device as recited in claim 17, characterized in that

the bond pad regions are present on the first side of the substrate, and

the substrate is a silicon substrate, that is patterned as required for access to the bond pad regions.

3. (*Currently Amended*) ~~A semiconductor device as claimed in Claim 1,~~ The semiconductor device as recited in claim 17, characterized in that a security layer is present at the second side of the substrate, which security layer leaves exposed the bond pad regions or any metallisation for access thereto.

4. (*Currently Amended*) ~~A semiconductor device as claimed in Claim 1,~~ The semiconductor device as recited in claim 17, characterized in that the bond pad regions are protected against probing with antiprobe means.

5. (*Cancelled*)

6. (*Cancelled*)

7. (*Currently Amended*) A carrier comprising a semiconductor device ~~according to Claim 1.~~ according to Claim 17.

Claims 8-10 (*Cancelled*)

Claims 11-16 (*Cancelled*)

17. (*Currently Amended*) ~~The semiconductor device as recited in claim 1,~~ A semiconductor device comprising a substrate with a first and an opposed second side, at

which first side a plurality of transistors and interconnects is present, which are covered by a protective security covering, which device is further provided with bond pad regions, characterized in that the protective security covering comprises a substantially non-transparent and substantially chemically inert security coating, the security coating including at least one layer of inorganic material, and the bond pad regions are accessible from the second side of the substrate,

wherein the security coating comprises,

a TiO_2 layer,

a coating layer based on monoAluminumPhosphate (MAP) filled with particles of either TiN or TiO_2; and

a multi alternating layer structure formed of Al and W layers, respectively.

18. (*Currently Amended*) ~~The semiconductor device as recited in claim 6,~~ A semiconductor device comprising a substrate with a first and an opposed second side, at which first side a plurality of transistors and interconnects is present, which are covered by a protective security covering, which device is further provided with bond pad regions, characterized in that the protective security covering comprises a substantially non-transparent and substantially chemically inert security coating, the security coating including at least one layer of inorganic material, and is formed of multiple alternate layers, which alternate layers are sensitive to different etchants and the bond pad regions are accessible from the second side of the substrate,

wherein the security coating comprises,

a TiO_2 layer,

a coating layer based on monoAluminumPhosphate (MAP) filled with particles of either TiN or TiO_2, and

a multi alternating layer structure formed of Al and W layers, respectively.

19. (*Currently Amended*) ~~The semiconductor device as recited in claim 1,~~ The semiconductor device as recited in claim 17, wherein the security coating is ~~either patterned or unpatterned.~~ is patterned.

20. (*Currently Amended*) ~~The semiconductor device as recited in claim 19,~~ The semiconductor device as recited in claim 17, wherein the security coating is patterned to provide capacitive coupling from the semiconductor device to an antenna structure in a carrier.

21. (*New*) The semiconductor device as recited in claim 19, wherein the security coating is patterned to provide capacitive coupling from the semiconductor device to an antenna structure in a carrier.